



Memory Bus

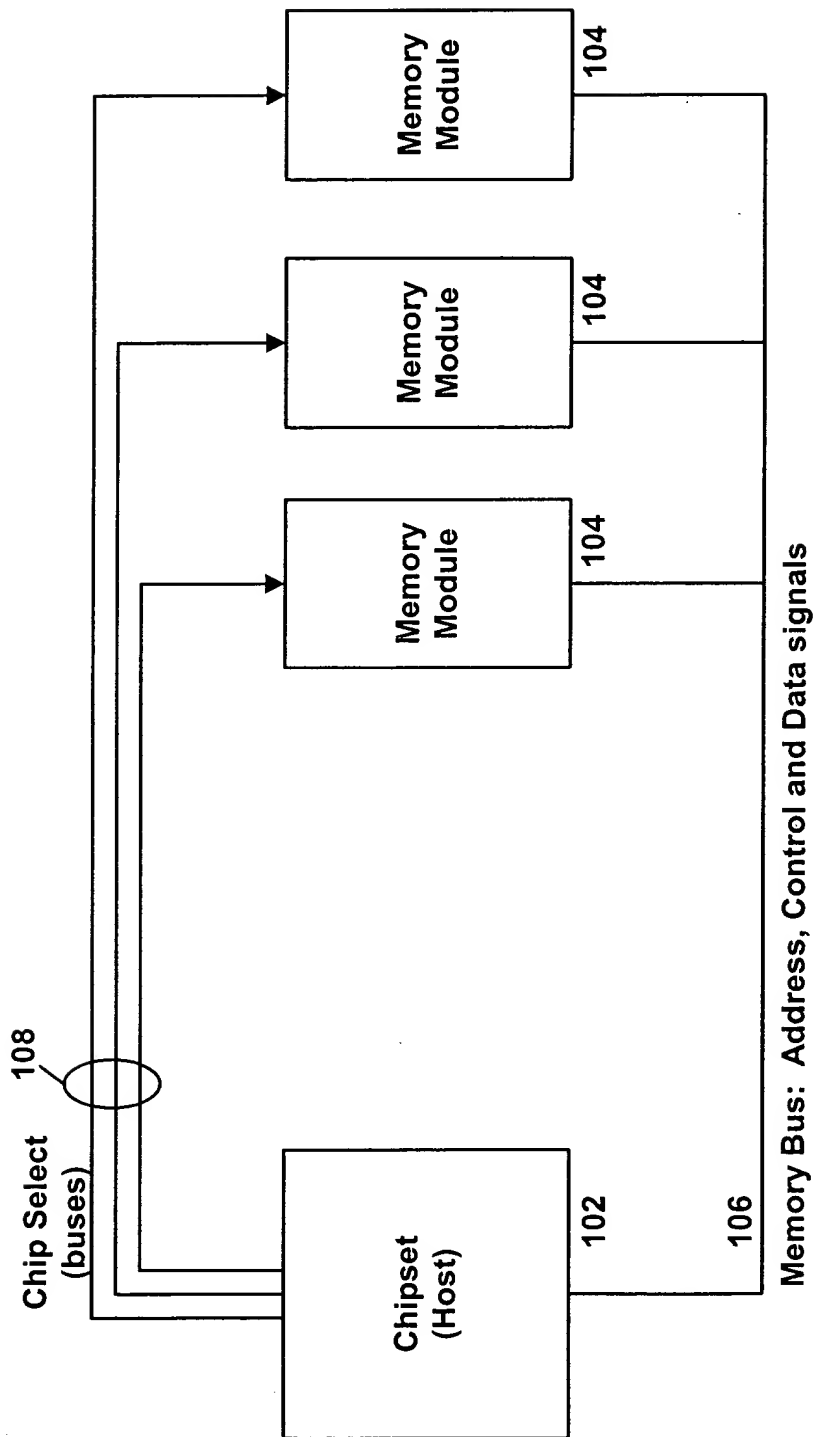


Figure 1
(Prior Art)

Memory Bus Peripheral (FPGA) Operation

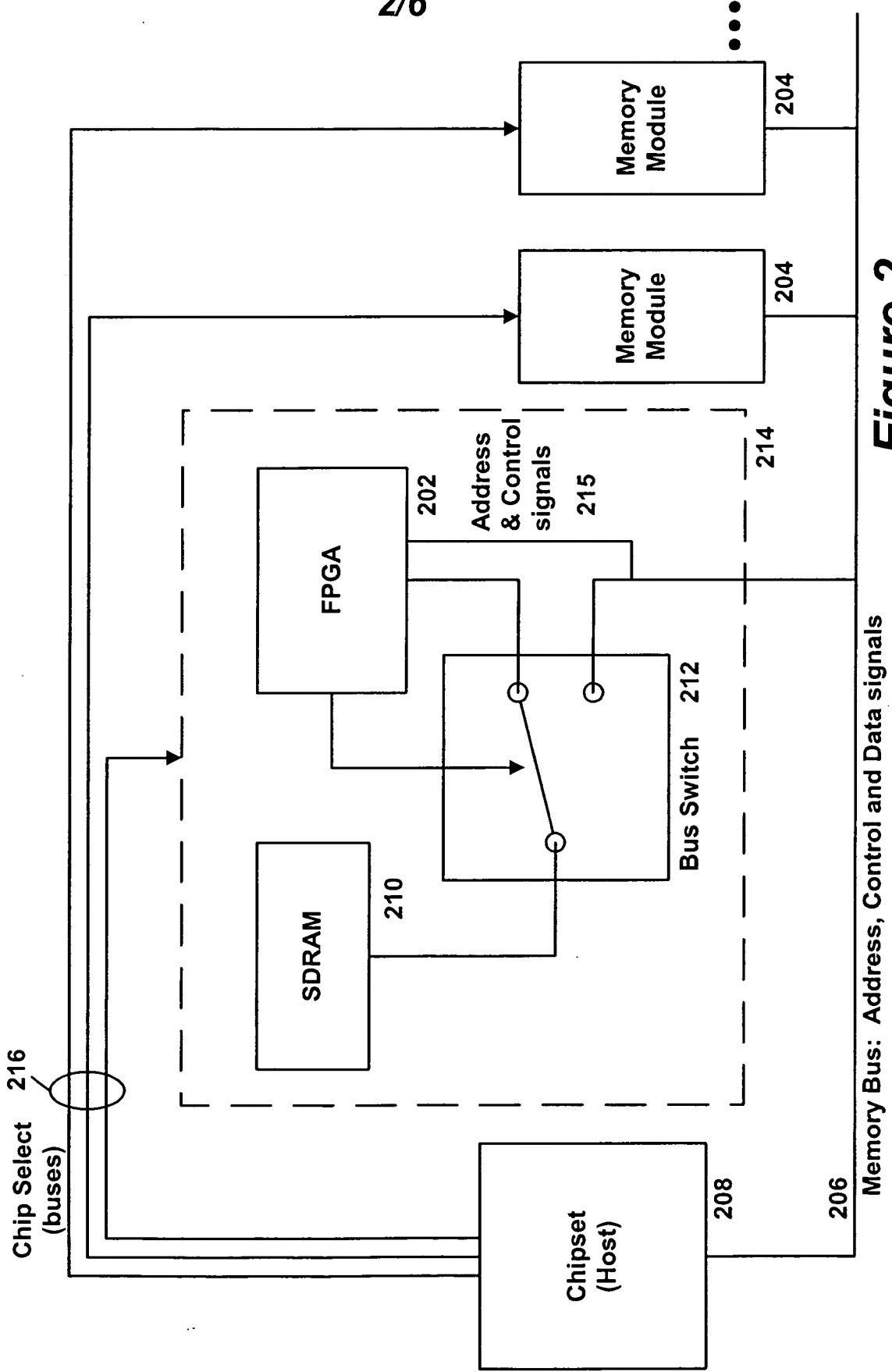


Figure 2

Operational Flowchart

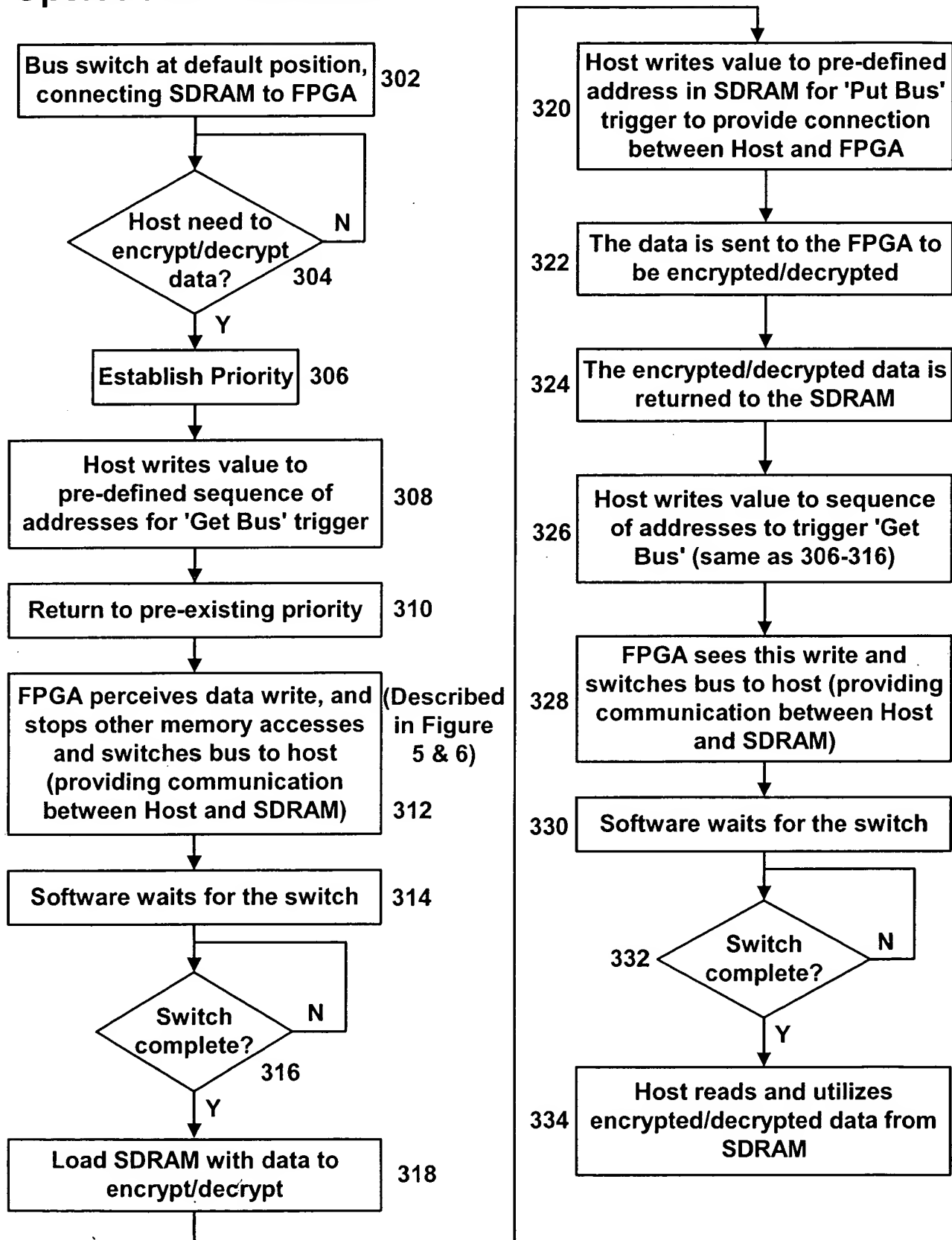


Figure 3

Example Memory Module Trigger Address Locations

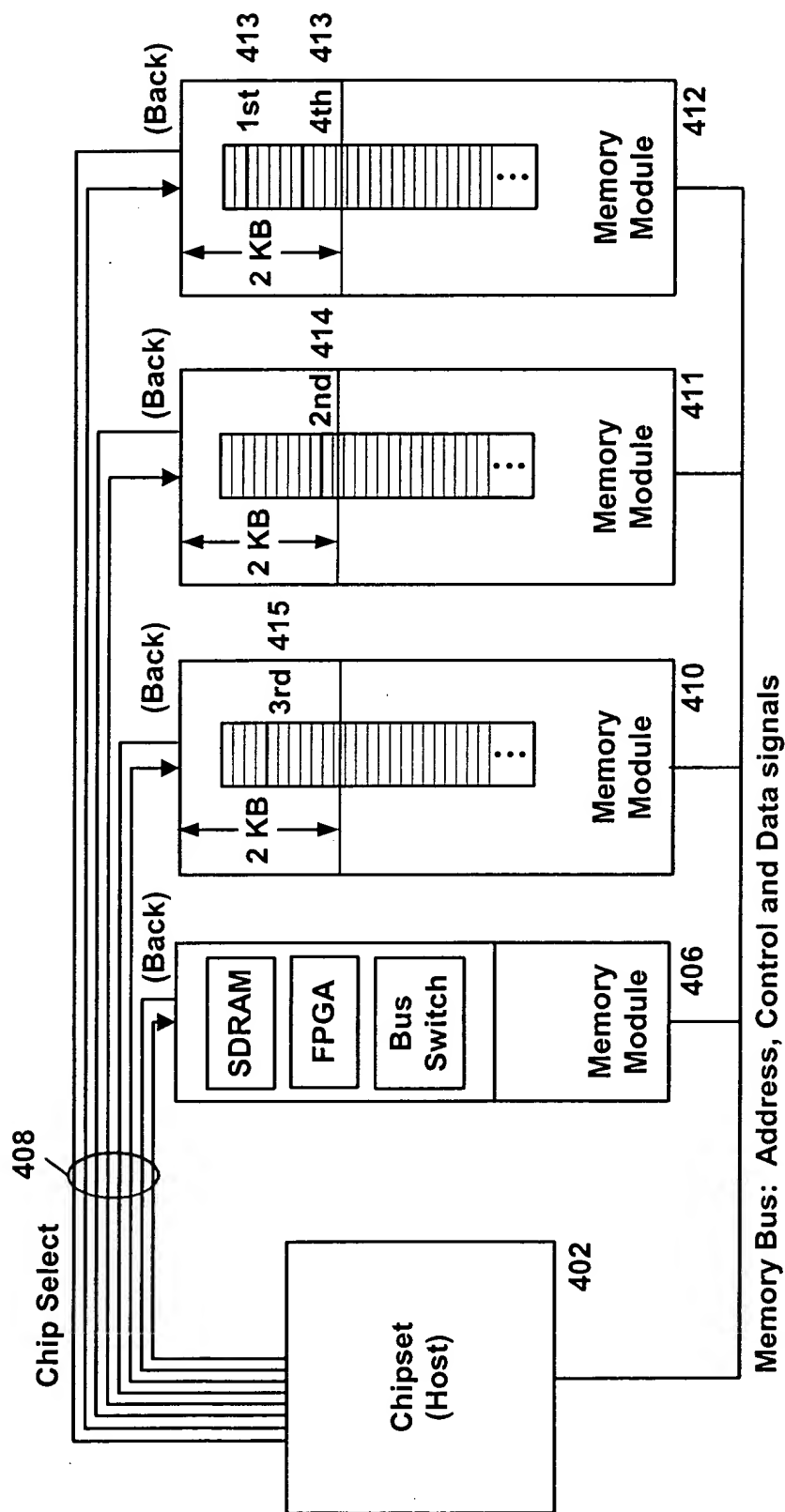
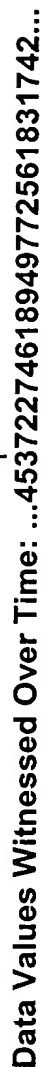


Figure 4

Data Values Witnessed Over Time: ...45372274618949762561831742....

Command Sequence: 57961

$N=5, K=5$



Command Sequence: 57961

N=5, K=5 | — 530



General Schematic of Data Value Sequence Detector

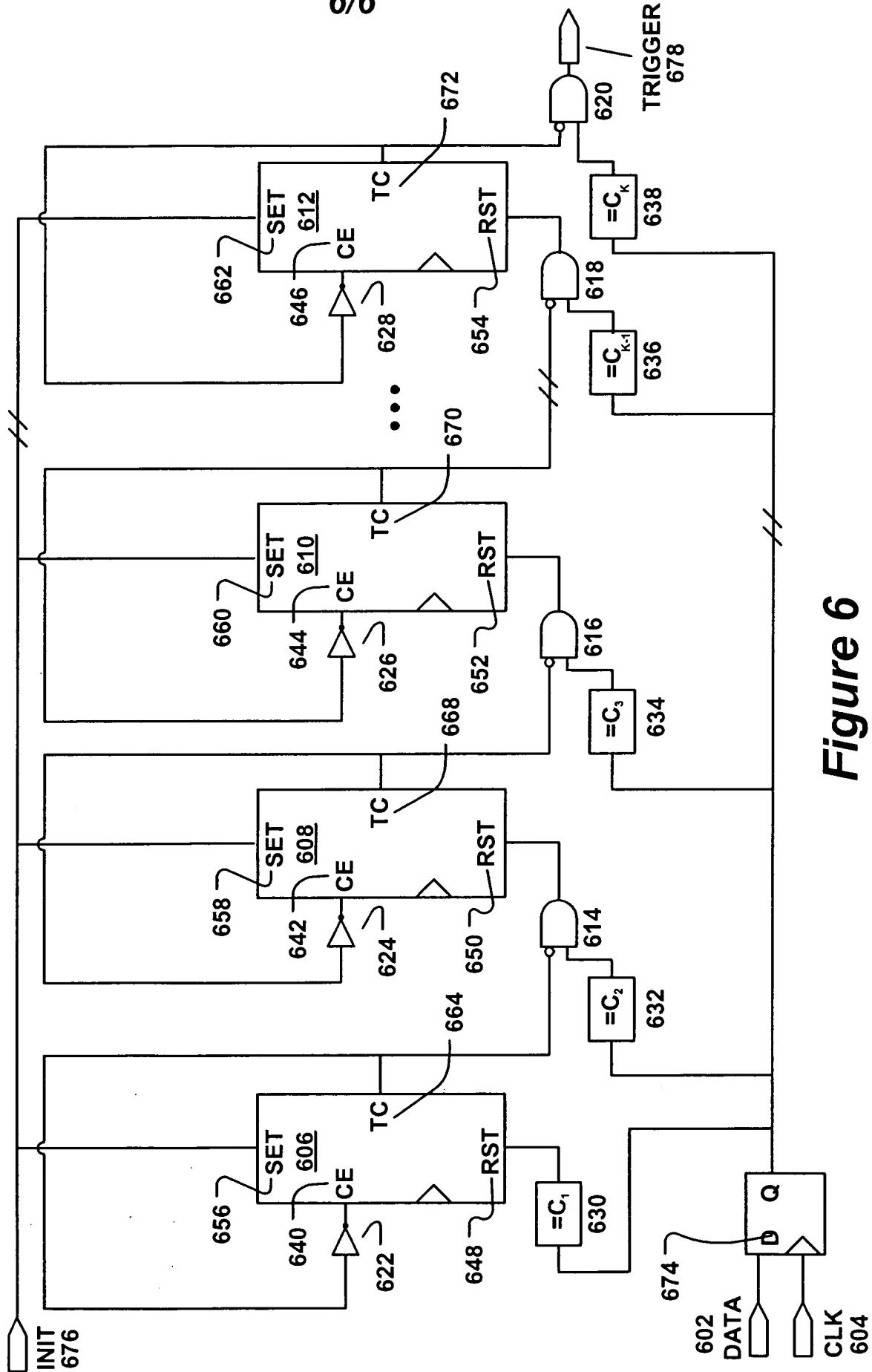


Figure 6